CLAIMS

1. A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

(a) forming a gate electrode on an insulating surface;

(b) depositing an insulating layer over the gate electrode and a region adjacent an edge of the gate electrode, such that the insulating layer comprises two outer surfaces which are substantially parallel to, and mutually spaced normally of, the insulating surface with a step extending therebetween;

(c) depositing a layer of semiconductor material;

(d) depositing a layer of electrode material;

(e) depositing a layer of negative resist material over the electrode material layer, the resist material being soluble in a predetermined solvent;

(f) irradiating the resist layer to render exposed portions insoluble in the predetermined solvent, the portion overlying the step being insufficiently exposed such that it remains soluble;

(g) developing the resist layer using the predetermined solvent, thereby removing the portion overlying the step; and

(h) removing the portion of the electrode material layer exposed by step (g) to define source and drain electrodes which extend over a respective one of the outer surfaces of the insulating layer to the step.

2. A method of Claim 1 wherein step (c) of depositing the semiconductor layer is carried out after step (h).

3. A method of Claim 1 wherein the edge of the gate electrode is substantially normal to the insulating surface.

4. A method of Claim 1 wherein a second thin film transistor is formed simultaneously with the first thin film transistor at an opposing edge of the gate electrode.

5. A method of Claim 1 wherein a low definition process is used to define one or more of the gate electrode and the layers.

6. A method of Claim 5 wherein a low definition process is used to define the gate electrode and the layers.

7. A method of Claim 1 wherein the semiconductor material comprises an organic material.

8. A method of Claim 1 wherein the height of the upper surface of the gate electrode above the substrate is in the range of 0.05 to 1.5 microns.

9. A method of Claim 1 including a further step after step (g) and before step (h) of subjecting the resist layer to a reflow process.

10. A method of Claim 1 including a further step after step (g) and before step (h) of subjecting the resist layer to an ashing process.